CLAIMS

What is claimed is:

1. A process for fabricating a contact structure in a silicon region in an integrated semiconductor circuit on a surface of a semiconductor wafer comprising:

depositing a dielectric layer over at least a portion of the silicon region;

etching a contact opening through the dielectric layer, the contact opening having a side wall and terminating in a bottom exposing a portion of the silicon region;

depositing a titanium metal layer within the contact opening covering the portion of the silicon region exposed by the bottom of the contact opening;

depositing an amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein on the side wall of the contact opening and over the titanium metal layer; and

filling at least a portion of the contact opening using a conductive material.

2. The process of claim 1, wherein depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein comprises a chemical vapor deposition process.

3. The process of claim 2, further comprising:

evacuating a deposition chamber to a pressure of less than about 100 torr;

heating the semiconductor wafer to a temperature in a range of about 200°C to about 600° C.; and

depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein using an organometallic precursor compound comprising tetrakis-dialkylamido-titanium in the deposition chamber by thermal decomposition thereof at or near the surface of the semiconductor wafer.

4. The process of claim 3, wherein the organometallic precursor compound comprises tetrakis-dimethylamido-titanium.

5. The process of claim 1, wherein the conductive material comprises a metal selected from the group consisting of tungsten, aluminum, copper and nickel.

6. The process of claim 1, wherein the conductive material comprises doped polycrystalline silicon.

7. The process of claim 1, further comprising:
forming a titanium silicide layer by heating the semiconductor wafer and reacting at least a portion of the titanium metal layer with the silicon region.

8. The process of claim 7, wherein the titanium silicide layer is formed prior to the depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride.

9. The process of claim 7, wherein the titanium silicide layer is formed subsequent to the depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride.

10. The process of claim 3, further comprising:
thermally processing the amorphous titanium carbonitride film in an atmosphere in the deposition chamber including one or more gases selected from the group consisting of nitrogen, hydrogen and the noble gases.

11. An integrated semiconductor circuit fabrication process for a contact structure in a silicon region in an integrated semiconductor circuit on a surface of a semiconductor wafer comprising:

depositing a dielectric layer over at least a portion of the silicon region;

etching a contact opening through the dielectric layer, the contact opening having a side wall and terminating in a bottom exposing a portion of the silicon region;

depositing a titanium metal layer within the contact opening covering the portion of the silicon region exposed by the bottom of the contact opening;

depositing an amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein on the side wall of the contact opening and over the titanium metal layer; and

filling at least a portion of the contact opening using a conductive material.

12. The process of claim 11, wherein depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein comprises a chemical vapor deposition process.

13. The process of claim 12, further comprising:

evacuating a deposition chamber to a pressure of less than about 100 torr;

heating the semiconductor wafer to a temperature in a range of about 200°C to about 600° C.; and

depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride therein using an organometallic precursor compound comprising tetrakis-dialkylamido-titanium in the deposition chamber by thermal decomposition thereof at or near the surface of the semiconductor wafer.

14. The process of claim 13, wherein the organometallic precursor compound comprises tetrakis-dimethylamido-titanium.

15. The process of claim 11, wherein the conductive material comprises a metal selected from the group consisting of tungsten, aluminum, copper and nickel.

16. The process of claim 11, wherein the conductive material comprises doped polycrystalline silicon.

17. The process of claim 11, further comprising:

forming a titanium silicide layer by heating the semiconductor wafer and reacting at least a portion of the titanium metal layer with the silicon region.

18. The process of claim 17, wherein the titanium silicide layer is formed prior to the depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride.

19. The process of claim 17, wherein the titanium silicide layer is formed subsequent to the depositing the amorphous titanium carbonitride film having substantially no crystalline titanium nitride.

20. The process of claim 13, further comprising:

thermally processing the amorphous titanium carbonitride film in an atmosphere in the deposition chamber including one or more gases selected from the group consisting of nitrogen, hydrogen and the noble gases.